Claims

1. A core cell fabricated upon a substrate of three columns of substrate material, the three columns of substrate material comprising a first n-type column, a first p-type column and a second n-type column, the p-type column being positioned between the first and second n-type columns.

2. The core cell of claim 1, wherein the bitline and complementary bitline are separated by one of at least a ground line and a voltage supply line.

3. A method for fabricating a core cell, the method comprising:

fabricating a substrate with a first column of p-type substrate material and two columns of n-type substrate material, the p-type substrate column being positioned between the two n-type substrate columns, each column being approximately equal in height and width;

fabricating two p-channel transistors on the p-type substrate;

fabricating at least 4 n-channel transistors, an equal number of n-channel transistors being fabricated on each n-type substrate;

coupling two n-channel and two p-channel transistors together to form two inverters; and

coupling the inverters and remaining transistors to form the core cell.

4. In a random access memory comprised of at least a plurality of core cells, a core cell, comprising:

first n-type substrate;

first p-type substrate; and

second n-type substrate, the first and second n-type substrates being positioned on opposite sides of the first p-type substrate.

5. The core cell of claim 4, wherein each substrate has a generally rectangular shape, the rectangles having substantially the same area.

6. The core cell of claim 4, wherein at least two PMOS transistors are fabricated on the first p-type substrate.

7. The core cell of claim 6, wherein at least 4 NMOS transistors are fabricated on the first and second n-type substrate.

8. The core cell of claim 7, wherein the two PMOS transistors and two NMOS transistors are coupled together to form two inverters, the two inverters being coupled together to form the core cell's storage element.

9. The core cell of claim 8, wherein at least a pair of bitlines are coupled to the core cell.

10. The core cell of claim 9, wherein the bitlines are separated by at least one of a voltage supply line and a ground voltage line, the bitlines not running in parallel immediately adjacent to one another.